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Gain–Bandwidth Limitations of Microwave Transistor Amplifiers

RODNEY S. TUCKER

Abstract—**Gain–bandwidth limitations of broad-band single-stage microwave transistor amplifiers are related to a simple transistor circuit model, to constraints on characteristic impedance in a distributed-element equalizer, and to the line lengths of this equalizer. The gain–bandwidth performance of commensurate distributed-element equalizers is compared with the performance of a lumped-element equalizer, and four distributed-element design examples are presented, including two commensurate equalizers and two computer-optimized networks.**

I. Introduction

STIMULATED by developments in microwave transistor technology, a number of authors have discussed the problem of broad-band microwave transistor amplifier design using computer-aided techniques [1], [2]. Recently, the work on broad-band impedance matching introduced by Fano [3], and extended by Youla [4] and other authors, has been applied to the synthesis of distributed commensurate equalizers for microwave transistor amplifiers [5]. This procedure relies upon certain approximate models of the transistor, but has proved successful in the design of single-stage and multistage amplifiers and in the problem of choosing an appropriate design with which to begin a computer-aided optimization scheme.

Manuscript received July 10, 1972; revised December 11, 1972. This work was supported by the Australian Radio Research Board.

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This paper extends the scope of work previously reported [5]. In Section II the gain–bandwidth limitations of a single-stage amplifier are related to a simple transistor circuit model, to constraints on the characteristic impedance in a distributed-element equalizer, and to the line lengths of this equalizer. The gain–bandwidth performance of commensurate distributed equalizers is compared with the performance of a lumped-element equalizer. In Section III it is shown that techniques introduced by Levy [6] for the synthesis of a ladder network with stub lengths different from those of the interconnecting lines may be used to advantage, this being illustrated in Section IV by an equalizer of improved gain–bandwidth performance. Gain–bandwidth limitations for a particular transistor are estimated in Section IV and some design examples are presented using both the direct synthesis method and a computer-aided technique. Theoretical and experimental results are compared.

II. Limitations on Amplifer Gain

The study of gain–bandwidth properties of a microwave transistor amplifier requires a suitable representation of transistor performance at frequencies approaching f_{max}, the maximum frequency of oscillation. Complex circuit models have been proposed [9], but are not readily suited to the problem. The work in this paper relies upon both an analytic or numerical model of transistor gain and a simple circuit model representing the output impedance of the transistor.

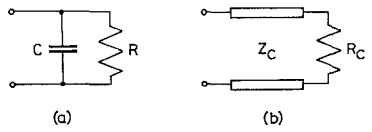

Fig. 1. Distributed circuit models of transistor output impedance. (a) Shunt capacitance and resistance. (b) Unit element and resistance.

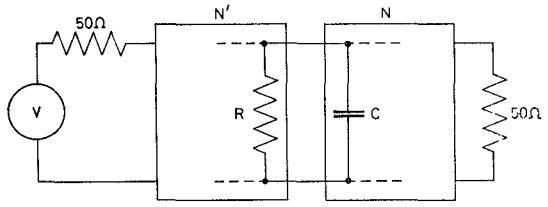

Fig. 2. Block schematic amplifier showing the distributed model of transistor output impedance.

Fig. 1 shows two simple distributed-element equivalent circuits for the output impedance of a microwave bipolar transistor in common emitter configuration or field-effect transistor in common source configuration. In each case the transistor is terminated with known source impedance. Accuracy of the models depends to some extent upon the particular transistor, but in most cases is sufficient to provide useful guidelines of gain–bandwidth. The present discussion is restricted to the model of Fig. 1(a).

The transformed frequency variable t is defined as

$$t = \Sigma + j\Omega = \tanh(s/4f_0) \tag{1}$$

where

$$s = \sigma + j2\pi f$$

and the frequency f has value f_0 when the unit elements (UE's) of a commensurate network each measure one-quarter wavelength. For given f_0 and specified termination at the input to the transistor, approximate values of R and C in Fig. 1(a) can be computed from measured scattering parameters of the transistor. If f_H is the upper frequency of the design passband and B_H is the capacitive susceptance of the transistor output admittance at that frequency, then

$$C = B_H/\Omega_H \tag{2}$$

where

$$\Omega_H = \tan(\pi f_H/2f_0).$$

In the region of f_{max} the gain of a transistor falls with increasing frequency at approximately 6 dB/octave [7]. If the transistor is fed from a specified source impedance which improves the input match at f_H, then this gain slope is modified slightly and the gain G is given by

$$G = G_H(f_H/f)^{x/3} \tag{3}$$

where G_H is the gain at $f=f_H$ and x is the rate at which gain falls with frequency in decibels/octave.

A single-stage amplifier is shown in Fig. 2 where N', representing a lossless input matching network and transistor, is fed from a 50-Ω source impedance. The distributed collector capacitance C is considered as part of the lossless distributed-element network N which is terminated with a 50-Ω load resistance. The overall amplifier is assumed to be stable.

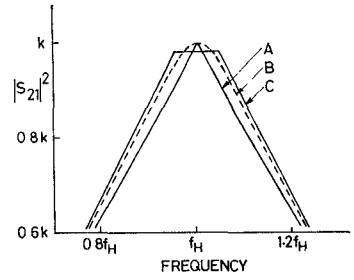

Fig. 3. $|S_{21}|^2$ against frequency.

Specifying an ideal amplifier transducer power gain to be constant for all frequencies from zero to f_H and to be zero at frequencies above f_H, the following is obtained:

$$\begin{aligned} |S_{21}(f)|^2 &= k(f/f_H)^{x/3}, && \text{for } f \le f_H \\ |S_{21}(f)|^2 &= 0, && \text{for } f > f_H \end{aligned} \tag{4}$$

where S is the scattering matrix of N, normalized to R at the input port and to 50 Ω at the output port, and where $k \le 1$. In the general case, where f_0 is not specified, approximation of this ideal $|S_{21}(f)|^2$ function with an appropriate realizable polynomial expression in t is an awkward problem. For this reason a simple approximation to $|S_{21}(f)|^2$ and numerical computations are used in the present discussion. Using the model of Fig. 1(a) and a simple commensurate distributed equalizer, it is assumed that $|S_{21}(\Omega)|^2$ is symmetrical about Ω_H. Curve A of Fig. 3 shows this $|S_{21}|^2$, while curve B is a realizable function differing significantly from curve A only in the region of f_H such that there are no abrupt changes of slope. Curve C is the approximation to curve B used in computations of gain–bandwidth.

Optimum amplifier gain is achieved by maximization of k. When $k=1$, the greatest value allowable for a passive equalizer, the output of the transistor is conjugately matched at the frequency f_H and mismatched at other frequencies. Further limitations on the value of k which result in mismatch at all frequencies are conveniently divided into two classes as follows.

A. Limitations Imposed by the Transistor

For the circuit model of Fig. 1(a) Fano [3] has shown that

$$\int_0^\infty \ln \frac{1}{|S_{11}(\Omega)|}\, d\Omega \le \frac{\pi}{RC} - \pi \sum_i a_i \tag{5}$$

where a_i are the zeros of S_{11} in the right half t plane and

$$|S_{11}(\Omega)|^2 = 1 - |S_{21}(\Omega)|^2. \tag{6}$$

Using (2) and putting $\sum_i a_i = 0$ for optimum utilization of gain–bandwidth, (5) becomes

$$\gamma \le 1/B_H R \tag{7}$$

where

$$\gamma = \frac{1}{\pi\Omega_H} \int_0^\infty \ln \frac{1}{|S_{11}(\Omega)|}\, d\Omega \tag{8}$$

which can be written as

$$\gamma = \frac{1}{2f_0\Omega_H} \int_0^{f_0} \{\sec^2(\pi f/2f_0)\} \cdot \ln \frac{1}{|S_{11}(f)|}\, df. \tag{9}$$

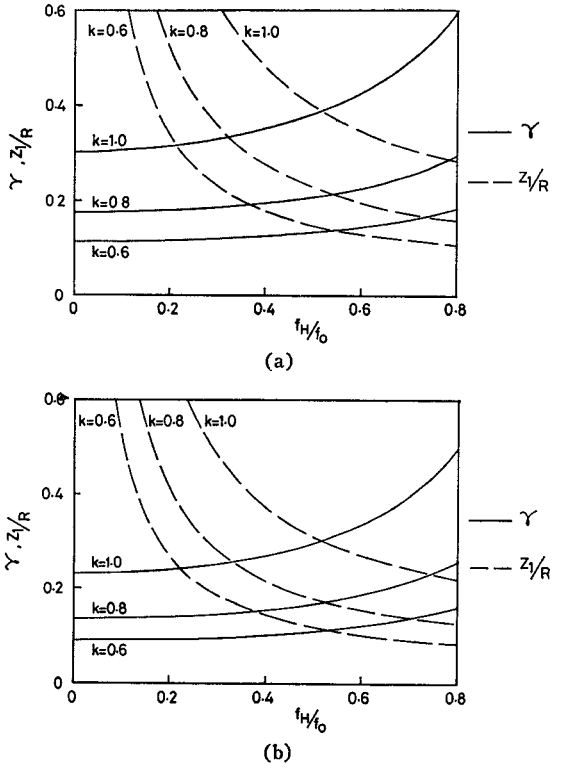

Fig. 4. γ and Z_1/R against f_H/f_0. (a) Transistor gain slope equals 4 dB/octave. (b) Transistor gain slope equals 6 dB/octave.

In Fig. 4 γ is plotted as a function of f_H/f_0, with k as a parameter, for transistor gain slopes of 4 and 6 dB/octave. A simple linear interpolation can be used to obtain values of γ at intermediate values of slope. If $1/B_HR$ for a given transistor is relatively small, restricting γ to a value less than the ordinate of the $k=1.0$ line at $f_H/f_0=0$, then maximum k is obtained at $f_H/f_0=0$. This corresponds to a lumped-element network, in which case all physical lengths are very much less than one wavelength. Larger values of f_H/f_0 result in reduced k, indicating that for increased line lengths of a commensurate distributed-element equalizer, gain–bandwidth limitations are more severe. If the B_HR product allows a value of γ to lie above the curve for $k=1$, extra capacitance must be connected in shunt with the output of the transistor which can be conjugately matched at f_H.

B. Limitations Imposed by Constraints on Characteristic Impedance of Equalizer Elements

Constraints on the realizable characteristic impedance of a transmission-line element play an important part in the design of microwave integrated circuits. Stripline characteristic impedance depends upon the substrate, but generally must be within the range 20–130 Ω. Now the optimum topology for an equalizer of the type considered here usually consists of a UE, connected to the collector of the transistor, followed by a series of stubs and further UE's connected in a ladder arrangement. The characteristic impedance of the first UE usually takes a more extreme value than does the characteristic impedance of any other element of the equalizer, suggesting that an investigation be made of the relation between this characteristic impedance and limitations of amplifier gain.

Fig. 5 shows the transistor model of Fig. 1(a) connected

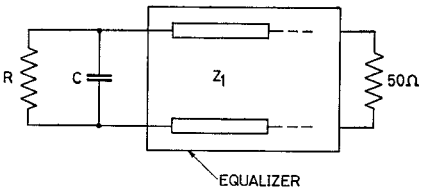

Fig. 5. Schematic diagram of equalizer, terminated with the circuit model of Fig. 1(a) at the input port and commencing with a UE of characteristic impedance Z_1.

to the equalizer. The first UE of the equalizer has a characteristic impedance of Z_1 and the impedance seen into this UE from the right is given by Z_l, where

$$Z_l(t) = Z_1 \cdot \frac{R + Z_1 t + RCZ_1 t^2}{Z_1 + (RCZ_1 + R)t}. \tag{10}$$

Using Youla's notation,

$$b(t) = \frac{R(CZ_1 + 1)t - Z_1}{R(CZ_1 + 1)t + Z_1}. \tag{11}$$

The impedance $Z_l(t)$ has one real, simple zero of transmission in Re $t>0$ at $t_0=\Sigma_0=1$ and one zero of transmission at $t_0=\infty$, and the first of these zeros in (11) gives

$$b(t_0) = \frac{R(CZ_1 + 1) - Z_1}{R(CZ_1 + 1) + Z_1}. \tag{12}$$

Youla's integral restrictions for a zero of order h in the right half-plane are (for real t_0 and nonconstant $|S_{11}(\Omega)|$)

$$\int_0^\infty \beta_r(t_0, \Omega) \ln |S_{11}(\Omega)|^2 \, d\Omega = b_r(t_0) - \eta_r(t_0),$$
$$r = 0, 1, \cdots, h-1 \tag{13}$$

where $\eta(t)$ is an all-pass function. For $h=1$, the required integral equation is obtained by substituting

$$\beta_r(t_0, \Omega) = \frac{(-1)^r}{2\pi} \cdot \frac{(t_0 + j\Omega)^{r+1} + (t_0 - j\Omega)^{r+1}}{(t_0^2 + \Omega_0^2)^{r+1}} \tag{14}$$

and $\eta(t)=1$ into (13) and taking the real part of both sides. Thus

$$\int_0^\infty \frac{\ln |S_{11}(\Omega)|^2}{1 + \Omega^2} d\Omega = \pi \ln \left| \frac{RCZ_1 + R - Z_1}{RCZ_1 + R + Z_1} \right| \tag{15}$$

which can be written as

$$\int_0^{f_0} \ln \frac{1}{|S_{11}(f)|} df = f_0 \ln \left| \frac{RCZ_1 + R + Z_1}{RCZ_1 + R - Z_1} \right|. \tag{16}$$

The other integral restriction, dependent upon the zero of transmission of $Z(t)$ at $t=\infty$, is identical to (9). Solutions for Z_1, normalized to R, are plotted in Fig. 4 as a function of f_H/f_0 and with k as a parameter, thus demonstrating limitations on k caused by constraints on Z_1. If f_H/f_0 has a small value, the gain–bandwidth as given by γ is near optimum, but Z_1 is large and may be unrealizable. On the other hand, for large values of f_H/f_0, Z_1 is small while γ is correspondingly large. Choice of the value of f_H/f_0 will depend upon the particular transistor but often involves some form of compromise.

III. Improved Amplifier Performance

Disadvantages of commensurate distributed equalizers can be explained in terms of relatively large physical dimensions compared with the lumped case [12] and in terms of gain–bandwidth performance. In Section II it was shown that lumped-element equalizers may exhibit superior performance, while similar conclusions can be drawn from the work of Carlin and Friedenson [8]. As distributed elements are generally easier to realize than lumped elements, it is profitable to examine a form of distributed network that shows some of the advantages of lumped-element networks. Considered here are ladder networks described by Levy [6] and consisting of a cascade of shunt stubs of equal length alternating with UE's each of twice the stub length. The approach may be used in the synthesis of an equalizer whose first UE is twice the length of other UE's and stubs.

Fig. 6(a) shows the first few elements of an equalizer synthesized by the usual commensurate network techniques. C_1 is the first t-plane capacitance, and Z_2 and Z_3 represent the first UE's of the equalizer. The method used to ensure that these UE's have equal characteristic impedances, enabling them to be considered as one UE, depends upon removal of t-plane capacitances before and after the UE's. Fig. 6(b) shows the first few elements of the equalizer with this done. The capacitance C represents partial removal of a pole, at $t=\infty$, of the admittance Y shown in Fig. 6(b), while C_R represents the remainder of the pole, extracted after the two UE's. It can be shown that for $Z_2 \geq Z_3$,

$$C_1 - C = \frac{Z_2 - Z_3}{Z_2(Z_2 + Z_3)} \tag{17}$$

and

$$Z_0 = (Z_2 + Z_3)/2. \tag{18}$$

The impedance represented by R, C_1, Z_2, and Z_3 in Fig. 6(a) has a zero of transmission of order 1 at $t=\infty$ and a zero of transmission of order 2 in Re $t>0$ at $t=1$. The three integral restrictions are

$$\frac{1}{2f_0\Omega_H}\int_0^{f_0}\{\sec^2(\pi f/2f_0)\}\cdot\ln\frac{1}{|S_{11}(f)|}\,df \leq \frac{1}{B_{HE}R} \tag{19}$$

$$\int_0^{f_0}\ln\frac{1}{|S_{11}(f)|}df = f_0\ln\left|\frac{RC_1Z_2 + R + Z_2}{RC_1Z_2 + R - Z_2}\right| \tag{20}$$

and

$$\int_0^{f_0}\{\cos(\pi f/f_0)\}\cdot\ln\frac{1}{|S_{11}(f)|}\,df = -f_0\cdot\frac{2RZ_2\{(Z_3 - Z_2) + Z_2C_1(Z_2 + Z_3)\}}{(Z_2 + Z_3)\{Z_2^2 - R^2(1 + Z_2C_1)^2\}} \tag{21}$$

where

$$B_{HE} = \Omega_H C_1.$$

Equation (19) can be written as

$$\gamma' \leq 1/B_H R \tag{22}$$

where

$$\gamma' = \gamma C_1/C. \tag{23}$$

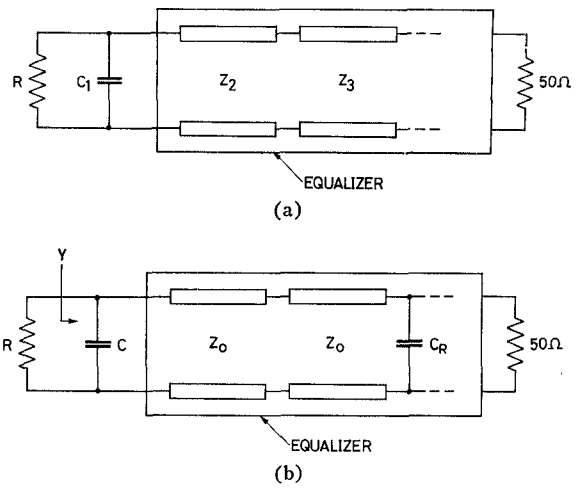

Fig. 6. Schematic diagram of equalizer. (a) Unequal characteristic impedances of first two UE's. (b) Equal characteristic impedances of first two UE's.

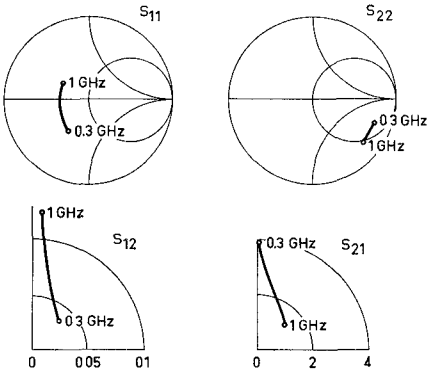

Fig. 7. Scattering parameter loci of the MT1061, with Smith chart representation for S_{11} and S_{22} and the usual complex plane representation for S_{12} and S_{21}.

Using the simple approximation to $|S_{21}|^2$ illustrated in Fig. 3, solutions for γ' and Z_0 are found to be almost identical to the previously computed values of γ and Z_1 for a given k and appropriate f_0, suggesting that the Levy-type equalizer has no inherent advantage over the simple commensurate type. The value of f_0 is almost twice that for a simple commensurate equalizer, however, and all elements except the first UE are consequently shorter. This enables more elements to be used for a given equalizer size, permitting greater flexibility in design. A particular example is outlined in the next section.

IV. Design Examples

The transistor considered here is an MT1061 with f_{max} of 3 GHz, somewhat less than that obtainable with more recent transistors. The form of the scattering parameters, shown in Fig. 7, is typical of higher frequency transistors, making the designs relevant while permitting measurements to be made below 1 GHz.

The first example is the design of a simple commensurate equalizer for a single-stage amplifier. The input matching network is shown cascaded with the transistor in Fig. 8 and the combined gain of the input matching network and transistor is found, by analysis, to have a slope of 5 dB/octave. This analysis also permits determination of parameters for

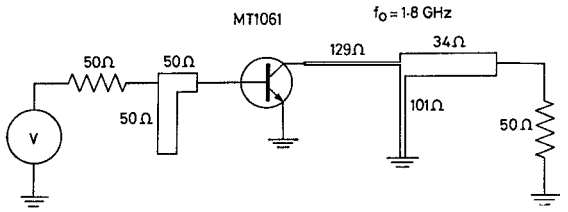

Fig. 8. Circuit of amplifier with commensurate equalizer, showing characteristic impedances of transmission-line elements.

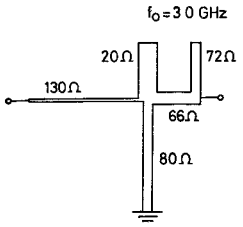

Fig. 9. Circuit of equalizer giving improved performance.

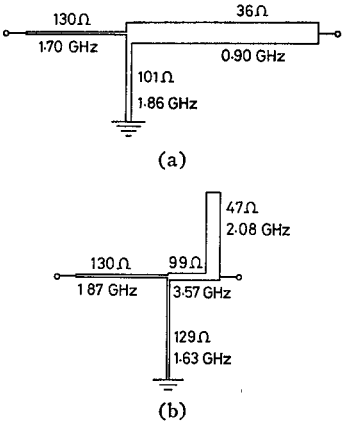

Fig. 11. Circuits of equalizers designed by optimization. Each transmission-line element is specified by characteristic impedance and by the frequency at which that element measures one-quarter wavelength. (a) Using the equalizer of Fig. 8 as a starting point. (b) Using the equalizer of Fig. 9 as a starting point.

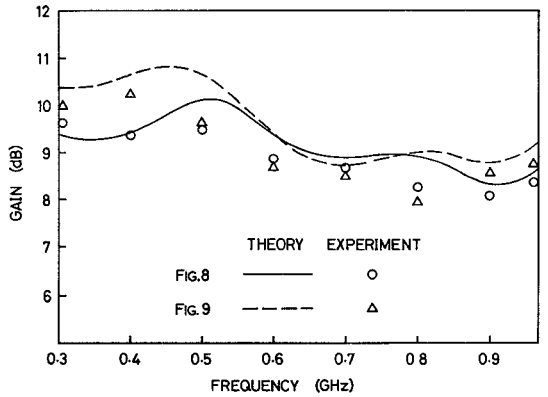

Fig. 10. Theoretical and experimental gain performance of the amplifiers of Figs. 8 and 9.

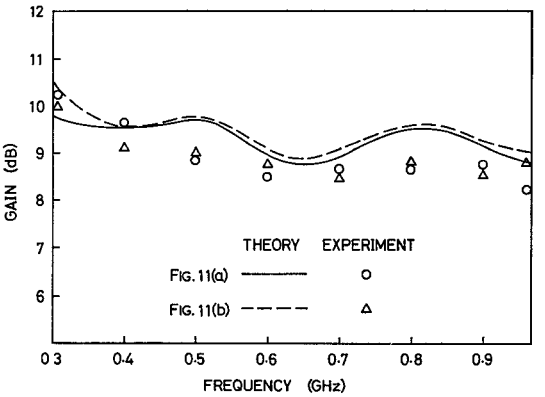

Fig. 12. Theoretical and experimental gain performance of the optimized amplifiers.

the model of Fig. 1(a). For $f_H = 1$ GHz these are $B_H = 0.35$ and $R = 13.4$ when normalized to 50 Ω. From (7) the gain–bandwidth limitation is

$$\gamma \leq 1/B_H R = 0.213. \tag{24}$$

Assuming that the upper limit of realizable characteristic impedance for a UE is 130 Ω,

$$Z_1/R \leq 0.194. \tag{25}$$

Referring to Fig. 4, $f_H/f_0 = 0.53$ and $k = 0.8$ satisfy both of these restrictions. With $f_H/f_0 = 0.53$, the optimum solution for k is 0.82 as found by an iterative scheme [5]. The synthesized equalizer is connected to the collector of the transistor, as in Fig. 8.

A second equalizer, designed for the same input matching network and transistor, is shown in Fig. 9. The first UE is twice the length of the other UE's, as described in Section III, and without significant increase in overall physical size, the equalizer has one more UE and shunt stub than the equalizer of Fig. 8. This permits the use of an $|S_{21}(f)|^2$ function with sharper cutoff rate above f_H. The gain is given by $k = 0.9$, representing a 10-percent improvement upon the first case. Fig. 10 shows the theoretical gain performance for both amplifiers, calculated by an independent direct analysis, and is compared with experimental results. These differ slightly from the experimental results of [5] due to improved accuracy of stripline construction.

Two noncommensurate equalizers, designed by a computer-aided technique based on Zangwill's modification of Powell's method [10] are illustrated in Fig. 11. The objective function is given by

$$U = 0.3(G_{\max} - \overline{G}) + \sum_{i=1}^{N} (G_i - \overline{G})^6 \tag{26}$$

where U is the objective function, $G_{\max}$ is the maximum available gain at $f = f_H$, G_i is the gain at one of N evenly spaced frequencies between 300 and 1000 MHz, and $\overline{G}$ is the average of all G_i. Minimization of U favors a flat overall gain, while ensuring that this gain is maximized. Parameter constraints, restricting the range of characteristic impedance to 20–130 Ω, are introduced by transformation [11]. The equalizers of Figs. 8 and 9 were used as starting points for optimization, and theoretical and measured gain of the optimized amplifiers is plotted in Fig. 12.

A comparison shows that the gain–bandwidth performance of the optimized noncommensurate networks is close to that

of the relevant commensurate networks, the main difference being a slight improvement in the "flatness" of gain. In both cases the equalizers designed by optimization have as their first element a UE of characteristic impedance equal to the specified upper limit. This is consistent with predictions made from gain–bandwidth theory applied to the commensurate case.

V. Conclusions

Within the limitations set by the use of approximate models of transistor behavior, a study has been made of the gain–bandwidth restrictions of a distributed-element equalizer with unspecified commensurate length. It has been shown that the greatest gain may be possible with a lumped-element equalizer, while simple commensurate networks can usually be expected to provide near optimum gain. The size problem associated with commensurate networks can be alleviated to some extent by the use of more specialized forms of network, but the problem is considerable in the case of FET's and other devices with high input and output impedance levels. With such devices constraints on characteristic impedance necessitate large equalizer line lengths which, in turn, have a detrimental effect on gain–bandwidth performance.

Acknowledgment

The author wishes to thank D. F. Hewitt for valuable discussions and guidance throughout the course of this work.

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Accurate Determination of Varactor Resistance at UHF and its Relation to Parametric Amplifier Noise Temperature

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Abstract—**A thorough investigation is made on the frequency-dependent properties of a varactor diode loss resistance at UHF. The variation of the losses with frequency in a varactor diode mounted cavity has been theoretically investigated, and it is shown that the previously reported inverse-squared frequency dependence of the varactor loss resistance can be attributed to the distributed cavity losses transformed across the varactor diode.**

A new measurement technique is introduced in which the circuit losses are first matched to the input line instead of the varactor loss resistance as an application of the relative impedance method. Measurements carried out with this technique for five different varactor diodes showed that the loss resistances of these diodes are not frequency dependent.

It is also shown that the choice of the varactor diode capacitance plays an important role on the parametric amplifier noise temperature at UHF. In an experimental parametric amplifier the effect of varactor diode capacitance on the noise temperature has been demonstrated. It has been theoretically and experimentally shown that, generally, varactor diodes having higher capacitances result in better noise temperature at UHF.

Manuscript received August 4, 1972; revised November 13, 1972. This work was supported in part by the Scientific and Technical Development Council of Turkey (TBTAK).

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I. Introduction

THE ACCURATE measurement of the varactor diode parameters has been the subject of many research workers for some time. The varactor diode parameters have been measured experimentally starting from lower side of UHF (that is, from 300 MHZ upwards) extending to X band and above. Different methods have been employed, each of which has distinct advantages over the others depending upon the frequency of measurement, components